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Attorneys for Plaintiff SYNOPSYS and Defendants AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-4669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

NOTICE OF SECOND REEXAMINATION AND CONSOLIDATION OF REEXAMINATION PROCEEDINGS

PLEASE TAKE NOTICE THAT, on April 19, 2006, the United States Patent Office granted the second petition for reexamination, filed on February 22, 2006, relating to the patent-in-suit, U.S. Patent No. 4,922,432. A copy of the order granting the February 22, 2006 petition for reexamination is attached hereto as Exhibit A. The Court should note that the second petition for reexamination was granted by the same patent examiner already handling the first reexamination filed on January 17, 2006 and granted on February 24, 2006. It is expected that these two granted re-examinations will now be merged together and formally assigned to the Examiner who granted the first request (St. John Courtenay III). *See* MPEP §2283 ("The two requests should be held in storage until the patent owner's statement and any reply by the requester have been received in Request 2, or until the time for filing same expires. Then, the TC Director or the TC Director's delegate will prepare a decision merging the two proceedings. . . . [T]he merged proceeding is returned to the Examiner immediately after the decision to issue an Office Action."). Applicable Patent Office Procedures provide that an Office Action will issue in the merged proceeding by **July 19, 2006**, one month from the expiration of Ricoh's time to respond to the latest-issued order. *See* MPEP §2261 ("If no submissions are made [by the patent owner in response to the order], the first action on the merits should be completed within *1 month* of any due date for such submission.").

Dated: May 1, 2006

Respectfully submitted,

HOWREY LLP

By: /s/Denise M. De Mory
Denise M. De Mory
Attorneys for Plaintiff
SYNOPSYS, INC. and for Defendants
AEROFLEX INCORPORATED,
AEROFLEX COLORADO SPRINGS,
INC., AMI SEMICONDUCTOR, INC.,
MATROX ELECTRONIC SYSTEMS,
LTD., MATROX GRAPHICS, INC.,
MATROX INTERNATIONAL CORP.,
and MATROX TECH, INC.

EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/007,945	02/22/2006	4922432		4490

24998 7590 04/19/2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Novak, Druce, DeLuca & Quigg LLP
1300 Eye St NW
Suite 400 East Tower
Washington, DC 20005

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/007,945*.

PATENT NO. *4922432*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/007,945	4922432	
	Examiner	Art Unit	
	St. John Courtenay III	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *22 February 2006* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO-1449, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

St. John Courtenay III
Primary Examiner
Art Unit: 3992

cc:Requester (if third party requester)

Response to Request for *ex parte* Reexamination

1. Reexamination has been requested for claims 13-17 of U.S. Patent number 4,922,432 ('432 patent).

2. A substantial new question of patentability affecting at least claim 13 of United States Patent number 4,922,432 is raised by the request for *ex parte* reexamination.

3. A prior art patent or printed publication raises a substantial new question (SNQ) of patentability where there is:

(A) a substantial likelihood that a reasonable Examiner would consider the prior art patent or printed publication **important** in deciding whether or not the claim is patentable, MPEP §2242 (I), and,

(B) the same question of patentability as to the claim has not been decided in a previous or pending proceeding or in a final holding of invalidity by a federal court. MPEP §2242 (III).

4. The '432 patent is currently assigned to:

RICOH COMPANY, LTD.
OHTA-KU
3-6, 1-CHOME NAKAMAGOME
TOKYO, JAPAN

5. The '432 patent application filing date was Jan. 13, 1988 and the patent issued on May 1, 1990. There is no claim to priority of record.

6. The Requester cites the following two publications by **KOWALKSKI** that have been previously addressed in related reexamination control No. 90/007,879: [1]

- **T.J. KOWALKSKI**, D.J. Geiger, W. H. Wolf, W. Fichtner, The VLSI Design Automation Assistant: From Algorithms to Silicon, IEEE Design & Test, pp. 33-43 (1985). (i.e., "**KOWALKSKI-85**")

- **Thaddeus Julius KOWALSKI**, The VLSI Design Automation Assistant: A Knowledge- Based Expert System, Carnegie-Mellon University PhD Thesis, April 1984. (i.e., "**KOWALKSKI-84**")

7. As set forth in the related 90/007,879 ORDER granting reexamination (mailed Feb. 24, 2006) the cited **KOWALKSKI-85** and **KOWALKSKI-84** publications were not of record in the file of the '432 patent and are not cumulative to the art of record in the original file.

8. In the request for reexamination, the Requester alleges that '432 patent claims 13-17 are either anticipated under 35 U.S.C. §102 or rendered obvious under 35 U.S.C. §103 in light of the following publications:

---

[1] See 90/007,879 PTO ORDER granting the Request for Reexamination of U.S. Patent number 4,922,432, mailed 24 Feb. 2006.

- Mitchell, T.M. et al., A Knowledge-Based Approach to Design, IEEE Trans. On Pattern Analysis and Machine Intelligence, Vol. PAMI-7, No. 5, Sept., 1985, pp. 502-510 (i.e., "**Mitchell-85**").

- Mitchell, T.M. et al., A Knowledge-Based Approach to Design, IEEE Workshop on Principles of Knowledge-Based Systems, Dec., 1984, pp. 27-34 ("**Mitchell-84**").

- U.S. Pat. No. 4,703,435 to Darringer et al. in view of **Mitchell-85**

- **KOWALKSKI-85** in view of **Mitchell-85.**

9. **MITCHELL-85** raises a SNQ of patentability.

The **MITCHELL-85** publication was not of record in the file of the '432 patent and is not cumulative to the art of record in the original file.

It is agreed that the **MITCHELL-85** publication would have been considered important by a reasonable Examiner in deciding whether or not at least claim 13 was patentable, for the reasons discussed *infra*.

As per independent claim 13:

Patent 4,922,432	**MITCHELL-85**
A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising:	Mitchell-85 teaches a computer-aided interactive process for designing an application specific integrated circuit that will perform a desired function [see Abstract, p. 502]. A user interacts with a knowledge-based VLSI expert editor, called VEXED, to design the circuit [page 503]. A prototype implementation of VEXED, known as VEXED.1, is described [page 503, n.1]. This prototype implementation is configured to execute on a Xerox Interlisp-D computer [page 504 n. 2; see also fig. 6, page 508]. Mitchell-85 teaches the process is module oriented. Initially, the user inputs the functions to be performed by the circuit which is represented at the highest level by a single "black box" module [page 503]. Mitchell-85 teaches the user and VEXED then iteratively refine this top-level module into sub-modules, representing the major functional blocks of the circuit. Each sub-module is then refined into sub-sub-modules, and so on, until the design is finished [page 503].

	Mitchell-85 teaches the functional specification of the highest-level "black box" module describes the inputs and outputs of this module, as well as the functions to be performed. See page 504. The functions are described in terms of actions and conditions. See page 504, describing the function of CAM-CELL in terms of actions and conditions.
storing a set of definitions of architecture independent actions and conditions;	Mitchell-85 teaches when the user elects to refine the highest-level "black box" module, a rule interpreter selects a set of rules embodying expert knowledge that "apply" to this module. See page 502, referring to "general rule interpreter," and page 504, describing example in which rules that apply to highest-level CAM-CELL module are selected. In deciding which rules apply, the rule interpreter interprets the specified function by applying a stored set of definitions of the possible actions and conditions. Mitchell-85 teaches, for example, Figure 1, (page 505), that shows the functional specification of the highest -level CAM-CELL module. In deciding the CAM-CELL module may be refined through application of a MEM-RULE, the rule interpreter interprets the function of the CAM-CELL, and decides

	that it includes outputting values that depend on the inputs at a previous time [page 504]. In interpreting this function, the rule interpreter applies a stored set of definitions of the actions and conditions specified in the function, for example, PREVIOUS, IF/THEN, GEQ (greater than or equal), EQUALS, NOT EQUALS, etc.
storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;	Mitchell-85 discloses that VEXED includes implementation rules that specify which "circuit structures can be used to implement what functions" [page 502]. These rules specify hardware cells to implement the specified functions, for example, a shift register for converting a serial signal to parallel, or figure-eight network for implementing an exclusive OR function: See Mitchell-85 at page 503 where the implementation rules are organized around a stored "taxonomy of modules (e.g., pass transistor networks, memories). At the lowest level, these modules represent "primitive circuit component" or hardware cells as indicated in fig. 6 at the top left column of page 508. Mitchell-85 teaches a specific example, illustrated in Fig. 5 (see page 507), in which the available hardware cells comprise an inverter loop, a pair of pass transistor networks, and a double-rail compare cell.

storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;	Mitchell-85 discloses a current implementation of VEXED that stores in an expert system knowledge base a set of implementation rules for selecting hardware cells to perform the specified actions and conditions, as shown on page 503, under "Knowledge of implementation methods," cont'd col. 2, through 1st paragraph. Mitchell-85 discloses an implementation of VEXED that stores in an expert system knowledge base a set of rules embodying tradeoff knowledge that selects between multiple implementations rules that apply to a particular module [see page 503, 2nd paragraph].
describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;	Mitchell-85 discloses that, in VEXED, the user describes the function to be performed by the circuit represented at the highest level by a single "black box" module [page 503]. The functions are described in terms of actions and conditions that are independent of any set architecture or technology [see page 503], describing the function of CAM-CELL in terms of actions and conditions. For example, Figure 1, (see page 505), that shows the functional specification of the highest-level CAM-CELL module. See also

	page 504, 2nd column, 2nd paragraph, line 13: "This function indicates that, at all times, the values of the output MATCH-J-OUT must equal some conditional expression based on the values of the inputs at that and previous times."
specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and	In interpreting the specified function of the highest-level "black box" module, the rule interpreter taught by Mitchell-85 specifies for each of the specified actions and conditions one of the stored definitions. For example, Mitchell-85 teaches when the user elects to refine the highest-level "black box" module, a rule interpreter selects a set of rules embodying expert knowledge that "apply" to this module. See page 502, referring to "general rule interpreter," and page 504, describing example in which rules that apply to highest-level CAM-CELL module are selected. In deciding which rules apply, the rule interpreter interprets the specified function by applying a stored set of definitions of the possible actions and conditions. Mitchell-85 teaches, for example, Figure 1, [page 505], that shows the functional specification of the highest -level CAM-CELL module.

selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit,	Mitchell-85 teaches that VEXED selects from the stored modules for each of the specified definitions a corresponding module which can be a hardware cell, e.g., shift register, figure-eight network, inverter loop, pass transistor network, double-rail compare cell, etc., for performing the desired function of the circuit. In the case where a module is selected, that module is then further refined through the process of Fig. 6 [page 508] until primitive circuit components, i.e., hardware cells, are reached.
said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base, and,	Mitchell-85 teaches that, in VEXED, a hardware cell is selected by applying to the specified definition a set of implementation rules and/or tradeoff rules stored in an expert knowledge base [see page 503, 2nd paragraph].
generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefore.	Mitchell-85 teaches that VEXED generates data structures that "describe the circuit, specifications associated with its whole and its parts, and a record of the desired plan of implementation choices resulting in the current design state" [page 503]. Mitchell-85 teaches that four types of objects are included. MODULES and

	DATAPATHS "describe circuit components and their interconnections, respectively." [page 503] Associated with each module is its FUNCTION [page 503]. Mitchell-85 teaches that associated with each DATAPATH is a DATASTREAM "which describes the signal values on that DATAPATH over time" [page 503]. Module FUNCTIONS "describe the mapping of input DATASTREAMS into output DATASTREAMS" [page 504].

10. **MITCHELL-84** raises a SNQ of patentability.

The **MITCHELL-84** publication was not of record in the file of the '432 patent and is not cumulative to the art of record in the original file. Because the **MITCHELL-84** publication is directed to the same VLSI Expert Editor "VEXED" ("VEXED" is an acronym **V**lsi **EX**pert **ED**ditor) as disclosed by **MITCHELL-85**, it is agreed that **MITCHELL-84** would have also been considered important by a reasonable Examiner in deciding whether or not at least claim 13 was patentable, for the same reasons discussed *supra* with respect to **MITCHELL-85**. [2]

[2] The Requester states on page 14 of the Request for Reexamination: "Mitchell85 is substantially similar to Mitchell84, so the following description will be in relation to Mitchell85, it being understood that the same description is possible in relation to

11. The Requester further alleges that a SNQ is raised under 35 U.S.C. §103 in light of **MITCHELL-85** in view of **Darringer** (U.S. Patent 4,703, 435).

Darringer (U.S. Patent 4,703, 435) is cited on the face of the '432 patent. The above request is therefore based at least in part on patents and/or printed publications already cited/considered in an earlier concluded examination of the patent being reexamined. On November 2, 2002, Public Law 107-273 was enacted. Title III, Subtitle A, Section 13105, part (a) of the Act revised the reexamination statute by adding the following new last sentence to 35 U.S.C. 303(a) and 312(a):

> "The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office."

For any reexamination ordered on or after November 2, 2002, the effective date of the statutory revision, reliance on previously cited/considered art, i.e., "old art," does not necessarily preclude the existence of a substantial new question of patentability (SNQ) that is based exclusively on that old art. Rather, determinations on whether a SNQ exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis.

In the present instance, because there exists a SNQ based solely on **MITCHELL-85**, as discussed *supra*, it is agreed that the proposed combination of **MITCHELL-85** in view of **Darringer** also raises a SNQ

Mitchell84." The Examiner concurs that the Mitchell85 and Mitchell84 publications are "substantially similar" because they disclose the same VLSI Expert Editor, "VEXED."

of patentability with respect to at least claim 13. A discussion of the specifics follows:

The Patent Owner admitted during prosecution that **Darringer** "does disclose a method and system for automatic logic design and it is known in the art of automatic layout to utilize cell libraries of circuit components." See paper No. 6 at 9. The Patent Owner distinguished **Darringer** solely on the basis that **Darringer** did not disclose an "architecture independent" functional specification input or a rule-based expert system for automatic logic synthesis. *Id.*

However, **MITCHELL-85** taught, to those of ordinary skill in the art at the time of the invention, a CAD tool that allows the designer to input a high level, architecture independent functional circuit description that is distinct from the register transfer level input taught in **Darringer**. See **MITCHELL-85**, at p. 504 and Fig. 1, p. 505. **MITCHELL-85's** teachings also include an expert system knowledge base of rules for iteratively refining circuit modules and selecting hardware cells. *Id.* at pp. 502-503.

Accordingly, the above-discussed teaching was not present during the prosecution of the application which became the '432 patent. Further, there is a substantial likelihood that this teaching would have been important to a reasonable examiner in deciding whether or not the claim is patentable.

12. **KOWALKSKI-85** in view of **Mitchell-85** raises a SNQ of patentability.

Because **KOWALKSKI-85** was previously found to have raised a SNQ with respect to at least claim 13 of related reexamination Control No. 90/007,879 [3] and also because **Mitchell-85** also raises a SNQ with respect to at least claim 13 (as discussed *supra*), it is agreed that the proposed combination of **KOWALKSKI-85** in view of **Mitchell-85** also raises a SNQ of patentability with respect to at least claim 13.

Accordingly, the above-discussed combined teaching of **KOWALKSKI-85** and **Mitchell-85** was not present during the prosecution of the application which became the '432 patent, nor was this combined teaching proposed in the related Request for Reexamination control No. 90/007,879. Further, there is a substantial likelihood that this new combined teaching would have been important to a reasonable examiner in deciding whether or not the claim is patentable.

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[3] See 90/007,879 PTO ORDER granting the Request for Reexamination of U.S. Patent number 4,922,432, mailed 24 Feb. 2006.

Conclusion

13. All claims are subject to reexamination.

14. Extensions of time under 37 C.F.R §1.136(a) will not be permitted in this proceeding because the provisions of 37 C.F.R. §1.136 apply only to "an Applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. §305 requires that *ex parte* reexamination proceedings "will be conducted with **special dispatch**" (37 C.F.R. §1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 C.F.R. §1.550(c).

15. The Patent Owner is reminded of the continuing responsibility under 37 C.F.R. § 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent number 4,922,432 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

How to Communicate with the USPTO

ALL correspondence relating to this *ex partes* reexamination proceeding should be directed as follows:

Please mail any communications to:

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Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed: ST. JOHN COURTENAY III PRIMARY EXAMINER

St. John Courtenay III (Monday – Friday 9:00 AM – 5:30 PM)
Primary Examiner
Central Reexamination Unit 3992
(571) 272-3761

Conferees:
SPRE CRU - 3992
CRU - 3992